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1 **A VLSI motion estimator for video image compression**
Chen-Mie Wu; Ding-Kuen Yeh;
Consumer Electronics, IEEE Transactions on , Volume: 39 Issue: 4 , Nov 1993
Page(s): 837 -846

[Abstract]   [PDF Full-Text (588 KB)] **IEEE JNL**

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2 **A real time MPEG2 main profile, main level motion-estimator chipset**
Pacalet, R.; Lafage, A.; Darbel, N.; Tychon, P.; Bellier, A.; Dejean, C.; Dutein, C. E.; Haas, S.; Laberl, S.; Lievre, B.; Simon, L.; Talayssat, J.;
Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC., 1
IEEE International , 6-8 Feb. 1997
Page(s): 260 -261, 469

[Abstract]   [PDF Full-Text (908 KB)] **IEEE CNF**

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3 **A quality measure for compressed image sequences based on an eye-movement compensated spatio-temporal model**
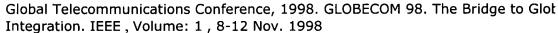*Westen, S.J.P.; Lagendijk, E.L.; Biemond, J.;*
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[Abstract]   [PDF Full-Text (516 KB)] **IEEE CNF**

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4 **Performance of motion estimators over MPEG coder considering frame analysis**
de Oliveira, G.C.; Alcaim, A.;

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Global Telecommunications Conference, 1998. GLOBECOM 98. The Bridge to Glok
Integration. IEEE , Volume: 1 , 8-12 Nov. 1998
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5 **One-dimensional full search motion estimation algorithm for video codi**
Chen, M.-J.; Chen, L.-G.; Chiueh, T.-D.;
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[Abstract]   [PDF Full-Text (440 KB)] **IEEE JNL**

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6 **Flexible VLSI architecture of motion estimator for video image compres**
Seung Hyun Nam; Moon Key Lee;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions
Volume: 43 Issue: 6 , June 1996
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7 **A cascading MRVQ-DCT scheme for the compression of sequence image**
Shih-Yu Huang; Jia-Shung Wang;
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Page(s): 1188 -1192

[Abstract]   [PDF Full-Text (408 KB)] **IEEE JNL**

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8 **Motion estimation using a complex-valued wavelet transform**
Magarey, J.; Kingsbury, N.;
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9 **An optimal quadtree-based motion estimation and motion-compensate**
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Schuster, G.M.; Katsaggelos, A.K.;
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10 **A simple recursive motion estimation technique for compression of HC signals**
de With, P.H.N.;
Image Processing and its Applications, 1992., International Conference on , 7-9 /
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11 **Multi-level pixel difference classification methods**
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12 **A programmable motion estimation processor for full search block matching**
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Acoustics, Speech, and Signal Processing, 1995. ICASSP-95., 1995 International
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13 **Spatial frequency based motion estimation for image sequence compression**
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14 **Low-complexity global motion estimation from P-frame motion vector: MPEG-7 applications**
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15 **Mesh based video coding at very low bitrate**
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2	☒	☐	US 6295546 B1	20010925	118
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4	☒	☐	US 6272178 B1	20010807	17
5	☒	☐	US 6240437 B1	20010529	138
6	☒	☐	US 6219688 B1	20010417	122
7	☒	☐	US 6173394 B1	20010109	124
8	☒	☐	US 6173305 B1	20010109	127
9	☒	☐	US 6116768 A	20000912	125
10	☒	☐	US 6101276 A	20000808	97
11	☒	☐	US 6098163 A	20000801	126

	Title	Current OR	Current XRef	Retrieval Classif
1	Long instruction word controlling plural independent processor operations	708/603		
2	Method and apparatus for eliminating the transpose buffer during a decomposed forward or inverse 2-dimensional discrete cosine transform through operand decomposition, storage and retrieval	708/402	708/401	
3	Method for choosing rate control parameters in motion-compensated transform-based picture coding scheme using non-parametric technique	382/239	348/416.1; 382/238; 382/250; 382/251	
4	Video data encoder and decoder	375/240.03	375/240.16; 382/232; 382/240; 382/246	
5	Long instruction word controlling plural independent processor operations	708/524	708/620	
6	Method, apparatus and system for sum of plural absolute differences	708/709	708/440; 708/670; 708/710; 712/200	
7	Instruction having bit field designating status bits protected from modification corresponding to arithmetic logic unit result	712/226	708/525; 712/221; 712/224	
8	Division by iteration employing subtraction and conditional source selection of a prior difference or a left shifted remainder	708/650	708/620	
9	Three input arithmetic logic unit with barrel rotator	708/236	708/209; 712/221	
10	Method and apparatus for performing two pass quality video compression through pipelining and buffer management	382/236		
11	Three input arithmetic logic unit with shifter	712/20		

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	Guttag, Karl M. et al.	☒	☐	☐	☐	☐	☐	☐	US 6370558	☐
2	Adiletta, Matthew J.	☐	☐	☐	☐	☐	☐	☐	US 6295546	☐
3	Chow, King-Wai et al.	☐	☐	☐	☐	☐	☐	☐	US 6292589	☐
4	Nieweglowski, Jacek et al.	☐	☐	☐	☐	☐	☐	☐	US 6272178	☐
5	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6240437	☐
6	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6219688	☐
7	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6173394	☐
8	Poland, Sydney W.	☐	☐	☐	☐	☐	☐	☐	US 6173305	☐
9	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6116768	☐
10	Adiletta, Matthew James et al.	☐	☐	☐	☐	☐	☐	☐	US 6101276	☐
11	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6098163	☐

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13	☒	☐	US 6058473 A	20000502	128
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21	☒	☐	US 5974539 A	19991026	140
22	☒	☐	US 5973742 A	19991026	27
23	☒	☐	US 5961635 A	19991005	138

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12	Rotation register for orthogonal data transformation	712/32	708/500	
13	Memory store from a register pair conditional upon a selected status bit	712/225	712/226; 712/234	
14	Long instruction word controlling plural independent processor operations	708/620	708/518; 708/628	
15	Data processing apparatus, system and method for if, then, else operation using write priority	712/226	712/225; 712/234	
16	Method and apparatus for eliminating the transpose buffer during a decomposed forward or inverse 2-dimensional discrete cosine transform through operand decomposition storage and retrieval	709/247	710/1; 710/29; 710/52; 710/58; 712/220	
17	Method, apparatus and system forming the sum of data in plural equal sections of a single data word	712/32	708/490; 708/500; 708/670	
18	Three input arithmetic logic unit with shifter and/or mask generator	712/221	708/209; 712/223	
19	Three input arithmetic logic unit capable of performing all possible three operand boolean operations with shifter and/or mask generator	712/221	708/230; 708/236	
20	Method and apparatus for interleaving and de-interleaving YUV pixel data	345/603	345/530; 345/555; 707/101; 711/157	
21	Three input arithmetic logic unit with shifter and mask generator	712/221	708/236; 712/224	
22	System and method for performing motion estimation with reduced memory loading latency	375/240.15	348/699; 375/240.24	
23	Three input arithmetic logic unit with barrel rotator and mask generator	712/221	708/230; 712/224	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
12	Balmer, Keith	☐	☐	☐	☐	☐	☐	☐	US 6067613	☐
13	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6058473	☐
14	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6032170	☐
15	Golston, Jeremiah E.	☐	☐	☐	☐	☐	☐	☐	US 6026484	☐
16	Adiletta, Matthew J.	☐	☐	☐	☐	☐	☐	☐	US 6026217	☐
17	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 6016538	☐
18	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5995748	☐
19	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5995747	☐
20	Biro, Larry Louis et al.	☐	☐	☐	☐	☐	☐	☐	US 5995080	☐
21	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5974539	☐
22	Gardyne, Robert et al.	☐	☐	☐	☐	☐	☐	☐	US 5973742	☐
23	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5961635	☐

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	Title	Current OR	Current XRef	Retrieval Classif
24	Apparatus and system for sum of plural absolute differences	712/221	708/236; 712/224	
25	Video encoder/decoder system	375/240.22	382/253	
26	Arithmetic logic unit with conditional register source selection	712/209	708/490	
27	Base address generation in a multi-processing system having plural memories with a unified address space corresponding to each processor	711/147	711/148; 711/152; 711/153	
28	Transparent block skipping in object-based video coding systems	382/243	382/239	
29	Long instruction word controlling plural independent processor operations	708/620	708/628	
30	Hardware branching employing loop control registers loaded according to status of sections of an arithmetic logic unit divided into a plurality of sections	712/221	712/223; 712/241	
31	Method, apparatus and system forming the sum of data in plural equal sections of a single data word	712/224	708/490; 708/518; 712/221; 712/36	
32	Address generator employing selective merge of two independent addresses	711/211	345/504; 345/572; 711/220	
33	Memory store from a selected one of a register pair conditional upon the state of a selected status bit	712/245	712/225	
34	Three input arithmetic logic unit with shifting means at one input forming a sum/difference of two inputs logically anded with a third input logically ored with the sum/difference logically anded with an inverse of the third input	712/221	708/209; 708/490; 712/223	
35	Method apparatus and system for correlation	708/525	712/221	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
24	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5960193	☐
25	Proctor, John J.	☐	☐	☐	☐	☐	☐	☐	US 5831678	☐
26	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5805913	☐
27	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5761726	☐
28	Lee, Ming-Chieh et al.	☐	☐	☐	☐	☐	☐	☐	US 5748789	☐
29	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5742538	☐
30	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5734880	☐
31	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5727225	☐
32	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5712999	☐
33	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐	US 5696959	☐
34	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐
35	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐

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	Title	Current OR	Current XRef	Retrieval Classif
36	Conditional processor operation based upon result of two consecutive prior processor operations	712/234	712/20	
37	Method for rounding using redundant coded multiply result	708/493		
38	Iterative division apparatus, system and method employing left most one's detection and left most one's detection with exclusive or	708/655		
39	Method, apparatus and system for multiply rounding using redundant coded multiply result	708/551	708/493	
40	Arithmetic logic unit having plural independent sections and register storing resultant indicator bit from every section	712/221	708/209; 708/230; 708/525; 708/670	
41	Three input arithmetic logic unit with controllable shifter and mask generator	708/230	712/200	
42	Packed word pair multiply operation forming output including most significant bits of product and other bits of one input	712/208	708/625	
43	Three input arithmetic logic unit with mask generator	712/36	345/501; 712/34	
44	Three input arithmetic logic unit forming mixed arithmetic and boolean combinations	708/670	708/236	
45	Iterative division apparatus, system and method employing left most one's detection and left most one's detection with exclusive OR	708/655		
46	Three input arithmetic logic unit with mask generator	712/36	345/501; 712/34	
47	Huffman encoding method, circuit and system employing most significant bit change for size detection	341/65		

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
36	Read, Christopher J.	☐	☐	☐	☐	☐	☐	☐		☐
37	Moyse, Philip et al.	☐	☐	☐	☐	☐	☐	☐		☐
38	Van Aken, Jerry R. et al.	☐	☐	☐	☐	☐	☐	☐		☐
39	Moyse, Philip et al.	☐	☐	☐	☐	☐	☐	☐		☐
40	Balmer, Keith et al.	☐	☐	☐	☐	☐	☐	☐		☐
41	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐
42	Balmer, Keith et al.	☐	☐	☐	☐	☐	☐	☐		☐
43	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐
44	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐
45	Van Aken, Jerry R. et al.	☐	☐	☐	☐	☐	☐	☐		☐
46	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐
47	Read, Christopher J. et al.	☐	☐	☐	☐	☐	☐	☐		☐

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48	☒	☐	US 5509129 A	19960416	
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50	☒	☐	US 5485411 A	19960116	
51	☒	☐	US 5479166 A	19951226	
52	☒	☐	US 5465224 A	19951107	
53	☒	☐	US 5446651 A	19950829	
54	☒	☐	US 5442581 A	19950815	
55	☒	☐	US 5420809 A	19950530	
56	☒	☐	US 5091782 A	19920225	

	Title	Current OR	Current XRef	Retrieval Classif
48	Long instruction word controlling plural independent processor operations	712/203	708/524; 712/24	
49	Three input arithmetic logic unit employing carry propagate logic	708/709		
50	Three input arithmetic logic unit forming the sum of a first input anded with a first boolean combination of a second input and a third input plus a second boolean combination of the second and third inputs	708/230		
51	Huffman decoding method, circuit and system employing conditional subtraction for conversion of negative numbers	341/65		
52	Three input arithmetic logic unit forming the sum of a first Boolean combination of first, second and third inputs plus a second Boolean combination of first, second and third inputs	708/236	708/670	
53	Split multiply operation	708/630		
54	Iterative division apparatus, system and method forming plural quotient bits per iteration	708/653	708/650	
55	Method of operating a data processing apparatus to compute correlation	708/200	708/445	
56	Apparatus and method for adaptively compressing successive blocks of digital video	348/400.1	375/240.16; 382/236; 382/239	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
48	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐
49	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐
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52	Guttag, Karl M. et al.	☐	☐	☐	☐	☐	☐	☐		☐
53	Moyse, Phillip et al.	☐	☐	☐	☐	☐	☐	☐		☐
54	Poland, Sydney W.	☐	☐	☐	☐	☐	☐	☐		☐
55	Read, Christopher J. et al.	☐	☐	☐	☐	☐	☐	☐		☐
56	Krause, Edward A. et al.	☐	☐	☐	☐	☐	☐	☐		☐